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EXAMINER	
VINH, LAN	

ART UNIT	PAPER NUMBER
1765	

DATE MAILED: 11/18/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/966,605	JIANG ET AL.	
	Examiner	Art Unit	
	Lan Vinh	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 September 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-2, 4, 7, 8 are rejected under 35 U.S.C. 102(e) as being unpatentable over Hung et al (US 6,380,096) in view of Hsieh et al (US 6,455,431)

Hung discloses an in-situ oxide etch process useful for copper dual damascene. This process comprises the steps of:

forming a low-k dielectric layer 14 over a silicon substrate 10/semiconductor body (col 2, lines 16-19)

forming a patterned photoresist/resist layer 98 over the low-k dielectric layer 14 (col 8, lines 66-67, col 9, lines 1-2, fig. 6)

performing an etching step 144 to etch the layer 14 using the photoresist pattern 98 (col 10, lines 26-28, fig. 6)

performing a post etch treatment 146 using oxygen plasma on the exposed dielectric layer 14 (as shown in fig. 9), the treatment step 146 and the etching step 144 are performed in the same chamber (col 10, lines 49-60), which reads on treating the low-k dielectric layer with a plasma, wherein the treating step occurs in-situ with respect to the etching step.

Unlike the instant claimed invention as per claim 1, Hung fails to disclose treating the low-k dielectric layer with a plasma having a bias power on the order of 400 W.

However, Hsieh discloses a resist stripping method comprises the step of treating a layer with a plasma having a bias power of about 400 W (col 4, lines 26-27)

Since Hung discloses using an inductive coupled high-density plasma etch reactor in his invention, one skilled in the art would have found it obvious to modify Hung's plasma treating step by using a plasma having a bias power of about 400 W as per Hsieh because Hsieh states that for an IPS (inductive plasma source) dielectric etch chamber, the substrate bias power applied typically ranges from about 100 W to about 400 W to obtain the bias the substrate bias voltage (col 3, lines 58-60; col 4, lines 25-27)

The limitations of using oxygen plasma, as recited in claims 2, 4, have been discussed above.

Regarding claim 7, Hung discloses that the post etch treatment strips/removes the remaining photoresist pattern (col 10, lines 48-50)

The limitation of claim 8 has been discussed above.

3. Claims 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hung et al (US 6,380,096) in view of Hsieh et al (US 6,455,431) and further in view of Tamaoka et al (US 6,232,237)

Hung as modified by Hsieh has been described above in paragraph 2. Unlike the instant claimed invention as per claim 3, Hung and Hsieh do not disclose that the plasma treatment comprises H_2O.

However, Tamaoka discloses a method for fabricating semiconductor device comprises the step of performing a plasma treatment using H_2O to remove a resist mask/pattern (col 5, lines 23-24)

Since Hung discloses the step of etching the dielectric layer 14 to form a opening/via before the plasma treatment step, one skilled in the art would have found it obvious to modify Hung and Hsieh step of plasma treatment to remove the resist by performing a plasma treatment using H_2O as per Tamaoka because Tamaoka states that by removing the resist mask using H_2O plasma, respective portions of the dielectric layer which are exposed on the inner side face of the via hole are neither adversely affected nor degraded (col 5, lines 37-41)

4 Claims 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hung et al (US 6,380,096) in view of Hsieh et al (US 6,455,431) and further in view of Lin et al (US 6,342,448)

Hung as modified by Hsieh has been described above in paragraph 2. Unlike the instant claimed invention as per claim 5, Hung and Hsieh fail to disclose using the low-k dielectric of organo-silicate glass (OSG) although Hung discloses using fluorinated silica glass (FSG) as the low k dielectric material (col 2, lines 33-34)

Lin, in a method of fabricating barrier adhesion to low-k dielectric layers, teaches that a low-k dielectric layer can be formed by fluorinated silica glass (FSG) or alternately by organo-silicate glass (OSG) (col 4, lines 6-15)

Hence, one skilled in the art would have found it obvious to substitute Hung and Hsieh FSG low k dielectric layer with organo-silicate glass (OSG) in view of Lin's teaching because both materials are equivalent low-k dielectric material, thus, the substitution of one for the other would have produced an expected result.

5. Claims 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hung et al (US 6,380,096) in view of Hsieh et al (US 6,455,431) and further in view of Cox (6,166,439)

Hung as modified by Hsieh has been described above in paragraph 2. Unlike the instant claimed invention as per claim 6, Hung and Hsieh fails to disclose using an ultra-low-k dielectric layer having a dielectric constant less than 2.5.

However, Cox discloses a method of application of low-k dielectric material comprises the step of forming a low-k dielectric material having a dielectric constant less than 2.0 (col 8, lines 48-50)

Hence, one skilled in the art would have found it obvious to modify Hung and Hsieh method by using a low-k dielectric material having a dielectric constant less than 2.0/ultra-low-k dielectric material which afford for facilitating the reduction of capacitive crosstalk between the adjacent conductive lines as taught by Cox (col 8, lines 50-52)

6. Claims 9-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hung et al (US 6,380,096) in view of Hsieh et al (US 6,455,431) and further in view of Yamazaki (6,350,701)

Hung as modified by Hsieh method has been described above in paragraph 2. Hung and Hsieh differ from the instant claimed invention as per claims 9-10 by performing the plasma treating step and the etching step in a same chamber instead of in separate chambers.

However, Yamazaki discloses an etching method comprises the step of performing the oxygen plasma treating step/ashing step and the etching step in separate chambers under vacuum (col 12, lines 6-32)

Hence, one skilled in the art would have found it obvious to modify Hung and Hsieh method by performing the oxygen plasma treating step/ashing step and the etching step in separate chambers as per Yamazaki because according to Yamazaki, it is particularly effective in a semiconductor manufacturing process in which cleanliness of an interface between films is important by providing an etching chamber, an ashing chamber as the reaction chamber in the system (col 3, lines 10-14)

7. Claims 11-12, 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hung et al (US 6,380,096) in view of Hsieh et al (US 6,455,431) and further in view of Lin et al (6,042,999)

Hung discloses an in-situ oxide etch process useful for copper dual damascene. This process comprises the steps of:

forming an etch stop layer 12 over a silicon substrate 10/semiconductor body (col 2, lines 16-17)

forming a dielectric layer 14 over the etch stop layer 12 (col 2, line 18, fig. 5), which reads on forming an interlevel dielectric (IDL) over the etchstop layer

forming a dielectric layer 20 over the dielectric layer 14 (fig. 5), which reads on forming an intrametal dielectric (IMD) over the IDL layer

forming a layer 94 over dielectric layer 20 (col 8, lines 60-61), which reads on forming a capping layer over the layer 20/IMD layer

forming a patterned photoresist/resist layer 98 having an opening on the layer 94/capping layer (col 8, lines 66-67, fig. 5)

performing an etching step 144 to etch the layers 20 and 14 using the photoresist pattern 98 as a mask (col 10, lines 26-28, fig. 6)

performing a post etch treatment 146 using oxygen plasma to strips/removes the remaining photoresist pattern (col 10, lines 48-50), the treatment step 146 and the etching step 144 are performed in the same chamber (col 10, lines 49-60), which reads on treating the low-k dielectric layer with a plasma, wherein the treating step occurs in-situ with respect to the etching step. It is noted that the applicants discloses that the cause of resist poisoning is believed to be the interaction between the resist and nitrogen-containing reagent from the low-k films in page 5 of the specification. Since Hung teaches the same step of removing the resist pattern using the same plasma treatment (oxygen) as the claimed invention, the plasma treatment is performed in the same chamber with the etching step 144 that etches a via in the same material (low-k dielectric) as the claimed invention, one skilled in the art would have found it obvious

that Hung 's oxygen plasma treatment step would have reduced poisoning by a nitrogen source as the claimed plasma treatment step.

completely filling the via with an antireflection coating (ARC) material 112 (col 9, lines 15-16, fig. 7), which reads on filling the via with an organic material

forming a trench pattern 118 over layer 20/IMD layer (col 9, lines 23-24, fig. 7)

etching a trench in the layer 20/IMD layer using the pattern 118 (col 9, lines 26-28)

removing the trench pattern 118 and organic material 112 in the via (col 9, lines 31-32)

removing the layer 94/capping layer and the exposed portion of etch stop layer 12 (col 9, lines 6-8, fig. 9)

filling the via and the trench with copper to form extending interconnect (col 9, lines 45-47)

Unlike the instant claimed invention as per claim 11, Hung fails to disclose that the plasma treatment occurs under a bias power of approximately 400 W.

However, Hsieh discloses a resist stripping method comprises the step of treating a layer with a plasma having a bias power of about 400 W (col 4, lines 26-27)

Since Hung discloses using an inductive coupled high-density plasma etch reactor in his invention, one skilled in the art would have found it obvious to modify Hung's plasma treating step by using a plasma having a bias power of about 400 W as per Hsieh because Hsieh states that for an IPS (inductive plasma source) dielectric etch chamber, the substrate bias power applied typically ranges from about 100 W to about 400 W to obtain the bias the substrate bias voltage (col 3, lines 58-60; col 4, lines 25-27)

Hung and Hsieh also differ from the instant claimed invention as per claim 11 by completely filling the via with an organic material instead of partially filling the via with an organic material.

However, Lin discloses a dual damascene process comprises the step of partially filling the hole/via 145 with ARC (antireflective coating)/organic material 150 (col 5, lines 36-64, fig. 2d)

Since both Hung and Lin are concerned with a method of forming dual-damascene structure having interconnect, one skilled in the art would have found it obvious to modify Hung and Hsieh method by partially filling the hole/via with organic material 150 as taught by Lin because Lin teaches that the partial filling of ARC serves its purpose of protecting the exposed substructure at the bottom of the hole/via from the damage that can be caused by the second etching energy to form conductive pattern (col 6, lines 10-14)

The limitations of claims 12 and 14 have been discussed above.

8. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hung et al (US 6,380,096) in view of Hsieh et al (US 6,455,431) and Lin et al (US 6,042,999) and further in view of Tamaoka et al (US 6,232,237)

Hung as modified by Hsieh and Lin has been described above in paragraph 7. Unlike the instant claimed invention as per claim 13, Hung, Hsieh and Lin do not disclose that the plasma treatment comprises H_2O.

However, Tamaoka discloses a method for fabricating semiconductor device comprises the step of performing a plasma treatment using H_2O to remove a resist mask/pattern (col 5, lines 23-24)

Since Hung discloses the step of etching the dielectric layer 14 to form a opening/via before the plasma treatment step, one skilled in the art would have found it obvious to modify Hung, Hsieh and Lin by performing a plasma treatment using H_2O as per Tamaoka because Tamaoka states that by removing the resist mask using H_2O plasma, respective portions of the dielectric layer which are exposed on the inner side face of the via hole are neither adversely affected nor degraded (col 5, lines 37-41)

9. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hung et al (US 6,380,096) in view of Hsieh et al (US 6,455,431) and Lin et al (US 6,042,999) and further in view of Yamazaki (6,350,701)

Hung as modified by Hsieh and Lin has been described above in paragraph 7. Hung, Hsieh and Lin differ from the instant claimed invention as per claim 15 by performing the plasma treating step and the etching step in a same chamber instead of in separate chambers.

However, Yamazaki discloses an etching method comprises the step of performing the oxygen plasma treating step/ashing step and the etching step in separate chambers under vacuum (col 12, lines 6-32, fig. 8).

Hence, one skilled in the art would have found it obvious to modify Hung, Hsieh and Lin by performing the oxygen plasma treating step/ashing step and the etching step in

separate chambers as per Yamazaki because according to Yamazaki, it is particularly effective in a semiconductor manufacturing process in which cleanliness of an interface between films is important by providing an etching chamber, an ashing chamber as the reaction chamber in the system (col 3, lines 10-14)

10. Claims 16-18 are rejected under 35 U.S.C. 102(e) as being unpatentable over Hung et al (US 6,380,096) in view of Hu (US 6,316,354)

Hung discloses an in-situ oxide etch process useful for copper dual damascene. This process comprises the steps of:

forming a low-k dielectric layer 14 over a silicon substrate 10/semiconductor body (col 2, lines 16-19)

forming a patterned photoresist/resist layer 98 over the low-k dielectric layer 14 (col 8, lines 66-67, col 9, lines 1-2, fig. 6)

performing an etching step 144 to etch the layer 14 using the photoresist pattern 98 (col 10, lines 26-28, fig. 6)

performing a post etch treatment 146 using oxygen plasma on the exposed dielectric layer 14 to remove the resist (col 10, lines 50-56 ; fig. 9), the treatment step 146 and the etching step 144 are performed in the same chamber (col 10, lines 49-60), which reads on treating the low-k dielectric layer with a plasma, wherein the treating step occurs in-situ with respect to the etching step.

Hung differs from the instant claimed invention as per claim 16 by treating the low-k dielectric with oxygen plasma to remove the resist instead of the hydrogen plasma to remove resist and reduce poisoning from a nitrogen source.

Hu discloses a process for removing resist mask comprises the step of treating the low-k dielectric layer with hydrogen plasma to reduce via poisoning from the resist removal (col 4, lines 26-50, col 5, lines 28-30)

Hence, one skilled in the art would have found it obvious to substitute Hung step of treating the low-k dielectric layer with oxygen plasma with hydrogen plasma to remove the resist because Hu states that via poisoning is avoided when the process to remove the via resist mask is carried out with a hydrogen plasma instead of conventional oxygen plasma (col 6, lines 37-41)

The limitations of claims 17-18 have been discussed above.

11. Claims 19-20 are rejected under 35 U.S.C. 102(e) as being unpatentable over Hung et al (US 6,380,096) in view of Hu (US 6,316,354) and further in view of Yamazaki (6,350,701)

Hung as modified by Hu has been described above in paragraph 10. Hung and Hu differ from the instant claimed invention as per claims 19-20 by performing the plasma treating step and the etching step in a same chamber instead of in separate chambers.

However, Yamazaki discloses an etching method comprises the step of performing the oxygen plasma treating step/ashing step and the etching step in separate chambers under vacuum (col 12, lines 6-32, fig. 8).

Hence, one skilled in the art would have found it obvious to modify Hung and Hu by performing the oxygen plasma treating step/ashing step and the etching step in separate chambers as per Yamazaki because according to Yamazaki, it is particularly effective in a semiconductor manufacturing process in which cleanliness of an interface between films is important by providing an etching chamber, an ashing chamber as the reaction chamber in the system (col 3, lines 10-14)

Response to Arguments

13. Applicants argue that since Hung teaches to perform the PET under zero/very low bias power, Hung teaches away from the claimed invention which uses a bias power on the order of 400 W. This argument is unpersuasive because what Hung teaches is to perform the PET at either zero bias power or at least one no more than 20% of the bias powers (1400 W) during the selective oxide etching step (col 10, lines 36-57, Table-5-continued). Thus, the examiner asserts that Hung does not teach away from using a bias power on the order of 400 W and the claimed invention is suggested by Hung. Accordingly, Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

14. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Conclusion

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lan Vinh whose telephone number is 703 305-6302. The examiner can normally be reached on M-F 8:30-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton, can be reached on 703 305-2667. The fax phone numbers for the organization where this application or proceeding is assigned are 703 872-9310 for regular communications and 703 872-9311 for After Final communications.

LV
November 11, 2003